Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Previously Presented) A method for testing an integrated circuit chip comprising:

a) applying a first reference voltage to a first input of a first monitor cell of at least one monitor cell integrated on the chip, wherein each of the monitor cells comprises a comparator and a latch coupled to the output of the comparator;

b) applying a first test voltage from a selected portion of the chip to a second input of the first monitor cell;

c) comparing the first reference voltage to the first test voltage using the comparator for providing a first result for storage in the latch of the first monitor cell;

d) applying a second reference voltage having a value different from the first reference voltage to the first input of the first monitor cell;

e) comparing the second reference voltage to the first test voltage using the comparator for providing a second result in the latch of the first monitor cell; and

f) analyzing the first and second results to determine a value for the first test voltage.

2. (Previously Presented) The method as recited in claim 1 further comprising adding a decoupling circuit to a selected portion of the chip based on the first and second results and repeating steps a) through f) after adding the decoupling circuit.

3. (Original) The method as recited in claim 1 further comprising applying sequentially the first reference voltage and the second reference voltage to a first input of a second of the at least one monitor cells and applying a second test voltage from a second selected portion of the chip to a second input of the second monitor cell.

4. **(Original)** The method as recited in claim 3 further comprising:

comparing the first reference voltage to the second test voltage using the comparator for providing a first result for storage in the latch of the second monitor cell;

comparing the second reference voltage to the second test voltage using the comparator for providing a second result in the latch of the second monitor cell; and

analyzing the first ands second results of the second monitor cell to determine a value for the second test voltage.

5. **(Original)** The method as recited in claim 4 further comprising analyzing the values determined for the first and second test voltages to determine a size and location for decoupling circuitry to be coupled to the chip.

6. **(Original)** The method as recited in claim 3 wherein the first and second test voltages are power supply voltages taken at different locations on the chip.

7. **(Original)** The method as recited in claim 1 wherein the second reference voltage is obtained by adjusting the first reference voltage to a new level.

8. **(Original)** The method as recited in claim 1 wherein testing is performed using automated test equipment and the first and second reference voltages are supplied by the ATE.

9. **(Original)** The method as recited in claim 1 wherein the testing is performed during the application of a scan chain to the chip.

10. **(Original)** The method as recited in claim 5 wherein the chip is a prototype chip and the decoupling circuitry is added to the design of the chip.

11. (Original) The method as recited in claim 1 wherein comparing the first reference voltage to the first test voltage and comparing the second reference voltage to the first test voltage comprises making a determination as to at least one of whether the first test voltage is less than the reference voltage when testing for undervoltage conditions or whether the first test voltage exceeds the reference voltage when testing for overvoltage conditions.

12. (Original) The method as recited in claim 1 wherein the comparing comprises making a determination as to whether the first reference voltage and the second reference voltage exceeds the first test voltage when testing for overvoltage conditions.

13. (Original) The method as recited in claim 1 wherein the comparing comprises making a determination as to whether the first reference voltage or the second reference voltage is less than the first test voltage when testing for undervoltage conditions.

14. (Previously Presented) A method of testing an integrated circuit comprising:

a) providing an overvoltage reference voltage and supply voltage to a first voltage comparator;

b) providing an undervoltage reference voltage and the supply voltage to a second digital comparator;

c) making a first determination for the first voltage comparator whether the overvoltage reference voltage exceeds the supply voltage;

d) making a second determination for the second comparator whether the supply voltage exceeds the undervoltage reference voltage; and

e) storing the first and second determinations in a first and a second latch attached respectively to the first and second comparators.

15. (Original) The method as recited in claim 14 further comprising adjusting the overvoltage reference voltage and the undervoltage reference voltage and repeating steps c) through e) and determining the value for the supply voltage from the stored results.

16. (Original) The method as recited in claim 15 further comprising duplicating each of the steps recited for claim 15 for a plurality of locations across the integrated circuit, each of the locations potentially having a different supply voltage than other of the locations.

17. (Original) The method as recited in claim 16 further comprising analyzing the values determined for the supply voltage to determine a size and location for adding decoupling circuitry.

18. (Cancelled)

19. (Currently Amended) ~~The integrated circuit as recited in claim 18,~~

An integrated circuit adapted for voltage level detection, the integrated circuit comprising:

a plurality of voltage supply conductors configured for providing a power supply voltage to the integrated circuit; and

a monitor cell integrated in the integrated circuit for testing over and under voltage conditions, the monitor cell comprising a first digital voltage comparator and a second digital voltage comparator each of the comparators coupled respectively to an associated latch for receiving the output of the voltage comparator, wherein:

inputs to the first comparator comprise a supply voltage from one of the plurality of supply conductors and an overvoltage reference voltage;

inputs to the second comparator comprise the supply voltage from the one of the plurality of supply conductors and an undervoltage reference voltage; and

wherein the monitor cell is further configured to receive at an input of the first comparator and at an input of the second comparator a reference voltage provided by one of the plurality of voltage supply conductors for comparison with the supply voltage.

20. (Currently Amended) ~~The integrated circuit as recited in claim 18,~~

An integrated circuit adapted for voltage level detection, the integrated circuit comprising:

a plurality of voltage supply conductors configured for providing a power supply voltage to the integrated circuit; and

a monitor cell integrated in the integrated circuit for testing over and under voltage conditions, the monitor cell comprising a first digital voltage comparator and a second digital voltage comparator each of the comparators coupled respectively to an associated latch for receiving the output of the voltage comparator, wherein:

inputs to the first comparator comprise a supply voltage from one of the plurality of supply conductors and an overvoltage reference voltage;

inputs to the second comparator comprise the supply voltage from the one of the plurality of supply conductors and an undervoltage reference voltage; and

wherein the monitor cell is configured to receive a reference voltage from automated test equipment and to transmit outputs of the associated latches to the automated test equipment.

21. (Currently Amended) ~~The integrated circuit as recited in claim 18,~~

An integrated circuit adapted for voltage level detection, the integrated circuit comprising:

a plurality of voltage supply conductors configured for providing a power supply voltage to the integrated circuit; and

a monitor cell integrated in the integrated circuit for testing over and under voltage conditions, the monitor cell comprising a first digital voltage comparator and a second digital voltage comparator each of the comparators coupled respectively to an associated latch for receiving the output of the voltage comparator, wherein the latches of monitor cell each include a timer configured to timestamp occurrences of overvoltage incidents and undervoltage incidents **and wherein:**

inputs to the first comparator comprise a supply voltage from one of the plurality of supply conductors and an overvoltage reference voltage; and

inputs to the second comparator comprise the supply voltage from the one of the plurality of supply conductors and an undervoltage reference voltage.